Electronic Version

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Claims

[c1] A circuit, comprising:

a control circuit adapted to generate at least a first and second signal in response to a test enable signal;

a differential driver circuit coupled to said control circuit, having a differential input node and a differential output node and adapted to receive a differential input signal at said differential input node, amplify said differential input signal and transmit a differential output signal onto said differential output node in response said first signal;

a programmable termination impedance circuit coupled to said control circuit and said differential output node, adapted to generate a differential termination impedance at said differential output node in response to said second signal; and

a differential receiver circuit coupled to said control circuit and said differential output node, adapted to receive said differential output signal, convert said differential output signal to a single ended signal and transmit said single ended signal in response to said test enable signal.

[c2] The circuit of claim 1 further comprising:

a first shift-register-latch circuit coupled to said differential input node and adapted to store said differential input signal; and
a second shift-register-latch circuit coupled to said differential receiver circuit and adapted to store said transmitted single ended signal.

[c3] The circuit of claim 1, wherein said differential driver circuit comprises:
a plurality of FIR latches coupled to said differential input node and adapted to store said differential input signal;
a plurality of preamplifier circuits coupled to said FIR latches and adapted to amplify said differential input signal, wherein said preamplifier circuits are enabled in response to said first signal;
a driver output stage coupled to said preamplifier circuits and adapted to transmit said differential output signal;
and a current DAC circuit coupled to said driver output stage and adapted to set drive strength of said driver output stage in response to a plurality of IDAC control signals.

[c4] The circuit of claim 3, wherein only one of said preamplifier circuits is enabled during a test sequence.

[c5] The circuit of claim 3, further comprising a third shift-

register-latch circuit coupled to said current DAC circuit and adapted to store said IDAC control signals.

[c6] The circuit of claim 1, wherein said programmable termination impedance circuit comprises a plurality of resistor components, each resistor component having an associated switch for selectively connecting that resistor component from a voltage source to said differential output node.

[c7] The circuit of claim 6, wherein at least one, but less than all of said resistor components are coupled to a first node of said differential output node and a remainder of said resistor components are coupled to a second node of said differential output node.

[c8] The circuit of claim 7, wherein said differential termination impedance is skewed at said first node and said second node when said test enable signal is active and said differential termination impedance is matched at said first node and said second node when said test enable signal is deactive.

[c9] The circuit of claim 7, wherein a first six of said resistor components are coupled to said first node and a second six of said resistor components are coupled to said second node.

[c10] The circuit of claim 9, wherein a first resistor of said first six resistor components is approximately 53 Ohms, a second resistor of said first six resistor components is approximately 71 Ohms, a third resistor of said first six resistor components is approximately 144 Ohms, a fourth resistor of said first six resistor components is approximately 287 Ohms, a fifth resistor of said first six resistor components is approximately 554 Ohms, a sixth resistor of said first six resistor components is approximately 3001 Ohms, a first resistor of said second six resistor components is approximately 53 Ohms, a second resistor of said second six resistor components is approximately 71 Ohms, a third resistor of said second six resistor components is approximately 144 Ohms, a fourth resistor of said second six resistor components is approximately 287 Ohms, a fifth resistor of said second six resistor components is approximately 554 Ohms, and a sixth resistor of said second six resistor components is approximately 3001 Ohms.

[c11] The circuit of claim 1, wherein said differential receiver circuit comprises:
a differential amplifier circuit coupled to said differential output node and adapted to receive said differential output signal;
a built-in offset voltage comparator circuit coupled to

said differential amplifier circuit and adapted to output a signal in response to said differential output signal and an offset voltage;

an output stage coupled to said differential amplifier circuit and said built-in offset voltage comparator circuit and adapted to transmit said single ended signal in response to said output signal of said built-in offset voltage comparator circuit; and

a level shifter circuit coupled to said output stage and adapted to transition power supply domains from an analog power supply domain to a digital power supply domain.

[c12] The circuit of claim 11, wherein said differential receiver further comprises a second built-in offset voltage comparator circuit electrically coupled in parallel with said first built-in offset voltage comparator circuit and adapted to output a signal in response to said differential output signal and a second offset voltage, wherein said first built-in offset voltage comparator circuit and said second built-in offset voltage comparator circuit form a hysteresis comparator.

[c13] The circuit of claim 12 wherein said hysteresis comparator is disabled when said second built-in offset voltage comparator circuit is disabled.

[c14] The circuit of claim 11, wherein said differential receiver circuit is disabled when said differential amplifier circuit is disabled.

[c15] The circuit of claim 11, wherein said output signal of said built-in offset voltage comparator is high when said received differential output signal is greater than said offset voltage and low otherwise.

[c16] A method of digitally testing a differential driver circuit, comprising:
activating a test enable signal;
skewing a differential output termination impedance in response to said test enable signal;
adjusting a voltage offset of a differential receiver circuit in response to said test enable signal;
selecting a power level for said differential driver circuit in response to said test enable signal, wherein said selected power level does not overpower said skewed output termination impedance;
enabling a decoder in response to said test enable signal, wherein said decoder activates only one segment of said differential driver circuit during a test sequence;
activating one of said segments for testing;
stimulating said differential driver circuit with digital test patterns;
receiving an output of said differential driver circuit by

said differential receiver circuit, wherein said differential driver output is in response to said digital test patterns;
converting said received differential driver output to a single-ended signal;
observing said single-ended signal; and
deactivating said test enable signal.

[c17] The method of claim 16, wherein said single-ended signal is observed by a shift-register-latch.

[c18] The method of claim 16, wherein said differential output termination impedance is skewed so that a first output termination impedance at a first output node of said differential driver circuit is greater than a second output termination impedance at a second output node of said differential driver circuit.

[c19] The method of claim 16, wherein said differential receiver circuit is powered on in response to said test enable signal when said test enable signal is active and said differential receiver circuit is powered off in response to a power down signal when said test enable signal is deactive.

[c20] A circuit, comprising:
means for generating at least a first and second signal in response to a test enable signal;

means for receiving a differential input signal, amplifying said differential input signal and transmitting a differential output signal onto a differential output node in response to said differential input signal and said first signal;

means for generating a differential termination impedance at said differential output node in response to said second signal; and

means for receiving said differential output signal, converting said differential output signal to a single ended signal and transmitting said single ended signal in response to said test enable signal.